[0179] FIG. **36** and FIG. **37** are sectional views, showing, in order, manufacturing steps of a semiconductor device according to Embodiment **11**. Firstly, manufacturing is carried out using the same procedure as in FIGS. **31**(*a*) to (*c*). Next, in FIG. **36**(*a*), the low concentration p-epitaxial layer **47** is epitaxially grown and embedded inside the deep trench **46**, in the same way as in FIG. **35**(*a*). After carrying out an etch back of the low concentration p-epitaxial layer **47**, as shown in the following FIG. **36**(*b*), the medium concentration p-layer **56** is epitaxially grown and embedded, as in FIG. **36**(*c*). Then, the medium concentration p-layer **56** is etched back, as shown in FIG. **36**(*d*), so that the heights of the upper surface of the medium concentration p-layer **56** and the upper surface of the n-type low concentration' region **42** are approximately the same. Subsequently, as shown in FIG. **37**(*a*), the high concentration p-layer **57** is epitaxially grown and embedded inside the deep trench **46**, forming the high concentration p-layer **57** on the surface of the medium concentration p-layer **56**. Then, as shown in FIG. **37**(*b*), a planarization of the surface is carried out using CMP, or the like. A final device form is as in FIG. **37** (*c*).

[0180] In the final device structure of FIG. **37**(*c*), the low concentration p-epitaxial layer **47** and the opposing n-type low concentration region **42** have approximate charge balance, and on the first main surface side, the n-type surface region **43** has approximate charge balance with the high concentration p-layer **57**. However, as a portion in which the medium concentration p-layer **56** and the opposing n-type low concentration region **42** are opposed becomes p-rich, thus preventing negative resistance, it. is possible to improve avalanche withstanding capability. The depth of the n-type surface region **43** is one-eighth or more, one-half or less, the depth of a whole parallel p-n layer portion having the first main surface as a reference. Also, the depths of the high concentration p-layer **57** and medium concentration p-layer **56** are one-eighth or more, one-half or less, the depth of the whole parallel p-n layer portion. As the portion in which the high concentration p-layer **48** and n-type low concentration region **42** are opposed in Embodiment 9 is replaced in Embodiment 11 with the portion in which the medium concentration p-layer **56** and n-type low concentration region **42** are opposed, the extent of p-richness in Embodiment 11 is lower than in Embodiment 9, thus improving the Eoff-turn off dv/dt trade-off.

[0181] As heretofore described, with the manufacturing method of Embodiment 11, it is possible to easily manufacture a device wherein improvements in Eoff-turn off dv/dt trade-off and avalanche withstanding capability are simultaneously achieved.

Embodiment 12

[0182] Main sectional views of manufacturing steps when using the manufacturing steps of the semiconductor device according to Embodiment 10 for the manufacturing steps of the semiconductor device according to Embodiment 8 are as in FIG. **38**. FIG. **38** is sectional views showing, in order, manufacturing steps of a semiconductor device according to Embodiment 12. Firstly, manufacturing is carried out using the same procedure as in FIGS. **31**(*a*) to (*c*). Next, the low concentration p-epitaxial layer **47** is epitaxially grown and embedded inside the deep trench **46**, as in FIG. **38**(*a*). Furthermore, as shown in FIG. **38**(*b*), a medium concentration p-layer **58** is epitaxially grown and embedded inside the low concentration p-epitaxial layer **47**. Continuing, as shown in FIG. **38**(*c*), a high concentration p-layer **59** is epitaxially grown and embedded inside the low concentration p-epitaxial layer **47**. Subsequently, as shown in FIG. **38**(*d*), a planarization of the surface is carried out using CMP, or the like. A final device form is as in FIG. **38** (*e*).

[0183] The invention not being limited to the heretofore described embodiments, various changes are possible. For example, the dimensions, concentrations, and the like, shown in the embodiments being examples, the invention is not limited to these values. Also, in each embodiment, the first conductivity type is taken to be the n-type and the second conductivity type taken to be the p-type, but the invention is established in the same way even when taking the first conductivity type to be the p-type and the second conductivity type to be the n-type. Also, the invention, not being limited to a MOSFET, can also be applied to an IGBT, a bipolar transistor, an FWD (free wheeling diode), a Schottky diode, or the like. Also, in Embodiment 3 to Embodiment 12, in the same way as in Embodiment 2, a configuration having a trench gate structure instead of a planar gate structure may be adopted.

INDUSTRIAL APPLICABILITY

[0184] As heretofore described, the semiconductor device according to the invention is useful as a high-power semiconductor device, and in particular, is suitable as a semiconductor device such as a MOSFET, IGBT, bipolar transistor, FWD, or Schottky diode, having a parallel p-n structure in a drift portion, wherein it is possible to balance an increase in breakdown voltage and an increase in current capacitance.

DESCRIPTION OF REFERENCE NUMERALS AND SIGNS

[0185] **1** n-type region
[0186] **2** p-type region
[0187] **3** p-base region
[0188] **4** n-type surface region
[0189] **5** p^+ contact region
[0190] **6** n^+ source region
[0191] **7** Gate insulating film
[0192] **8** Gate electrode
[0193] **9** Interlayer insulating film
[0194] **10** Source electrode
[0195] **11** n^+ drain region
[0196] **12** Drain electrode
[0197] **20** Parallel p-n layer
[0198] **21** n-type high concentration region
[0199] **22** n-type low concentration region

1. A semiconductor device, characterized by comprising:
an active portion provided on a first main surface side;
a low resistance layer provided on a second main surface side;
a parallel p-n layer, provided between the active portion and low resistance layer, wherein a first conductivity type region and second conductivity type region are disposed alternately;
a second conductivity type base region, provided on the first main surface side of the second conductivity type region, that has an impurity concentration higher than that of the second conductivity type region; and
a first conductivity type high concentration region, provided on the first main surface side of the first conductivity type region, that is positioned farther to the second main surface side than an end portion on the second main surface side of the second conductivity type base region, and has an impurity concentration higher than an impurity concentration on the second main surface side of the first conductivity type region.